WE CLAIM:

1. A semiconductor device comprising:
   a semiconductor chip having a planar active surface including an integrated circuit, said circuit having metallization patterns including a plurality of contact pads;
   each of said contact pads having an added conductive layer on said metallization, said added layer having a conformal surface adjacent said chip and a planar outer surface, said outer surface suitable to form metallurgical bonds without melting.

2. The device according to Claim 1 wherein said chip metallization is aluminum, copper, or alloys thereof.

3. The device according to Claim 1 wherein said conductive layer consists of at least two conductive sub-layers, one being a conductive diffusion barrier, the other, outer layer being bondable.

4. The device according to Claim 3 wherein said conductive diffusion barrier is selected from a group consisting of nickel, vanadium, titanium, tungsten, tantalum, osmium, chromium, and aluminum.

5. The device according to Claim 3 wherein said bondable layer is selected from a group consisting of gold, palladium, platinum, silver, and alloys thereof.

6. The package according to Claim 1 wherein said outer surface has a flatness suitable for metal interdiffusion with another flat surface formed by a metal suitable for interdiffusion.

7. The device according to Claim 1 further comprising:
   a distribution of said contact pads such that an

area portion of said active chip surface is available for attaching a thermally conductive plate, said plate having a thickness compatible with the thickness of said conductive pad layer.

8. The device according to Claim 7 wherein said plate has an outer surface suitable for metallurgical bonds.

9. The device according to Claim 8 wherein said plate surface is solderable.

10. The device according to Claim 7 wherein said contact pads are arrayed along the periphery of said chip and said plate is located inside said periphery.

11. The device according to Claim 7 wherein said contact pads are arrayed in the center of said chip and said plate is formed as a frame around said contact pads.

12. The device according to Claim 1 wherein said semiconductor chip is made from a material selected from a group consisting of silicon, silicon germanium, gallium arsenide, and any other semiconductor material used in integrated circuit fabrication.

13. The device according to Claim 1 further comprising encapsulation material protecting at least the chip surface opposite said active surface.

14. The device according to Claim 13 wherein said encapsulation material is a molding compound.

15. The device according to Claim 1 further comprising a metallic or insulating substrate having terminal pads aligned with the distribution of said chip contact pads, each terminal pad being bonded to one of said chip contact pads having said added layer, respectively, such that electrical contact between said chip and said substrate is established, while forming a gap therebetween having a width of

approximately said added layer thickness.

16. The bonding according to Claim 15 wherein said bonding is selected from a group of techniques and materials comprising:

direct welding by metallic interdiffusion;

attachment by solder paste; and

attachment by conductive adhesive.

17. The device according to Claim 15 further comprising encapsulation material protecting at least the chip surface opposite said active surface and filling said gaps.

18. The device according to Claim 17 further comprising a substrate addition suitable for attaching said device to a board, said addition selected from a group consisting of solder balls, conductive lands, and bondable surface finish.

19. The device according to Claim 1 further comprising a protective layer on the chip surface opposite said active surface, said protective layer shielding against light and disturbing environmental influences.

20. The device according to Claim 19 wherein said protective layer comprises hardened polymeric material.

21. A semiconductor assembly comprising:

a semiconductor chip having a planar active surface including an integrated circuit, said circuit having metallization patterns including a plurality of contact pads, each of said contact pads having an added conductive layer on said metallization, said added layer having a conformal surface adjacent said chip and a planar outer surface, said outer surface suitable to form metallurgical bonds without melting; and

an assembly board having a plurality of planar, metallurgically bondable terminal pads in a distribution aligned with the distribution of said chip contact pads;

said chip metallurgically bonded to said board so that each of said chip contact pads is connected to a corresponding board terminal pad.

22. The assembly according to Claim 21 wherein said assembly board is selected from a group consisting of organic materials, including FR-4, FR-5, and BT resin, with or without strengthening or thermally modulating fibers; metals; and ceramics.

23. The assembly according to Claim 21 wherein said board terminal pads comprise an outer surface selected from a group consisting of gold, palladium, silver, platinum and alloys thereof.

24. The assembly according to Claim 21 wherein said metallurgical bonding of said outer layer surface of said contact pads to said terminal pads is selected from a group of techniques and materials comprising:

direct welding by metallic interdiffusion;

attachment by solder paste; and

attachment by conductive adhesive.

25. A semiconductor assembly comprising:

a semiconductor chip having a planar active surface including an integrated circuit, said circuit having metallization patterns including a plurality of contact pads, said contact pads distributed such that an area portion of said chip surface is available for attaching a thermally conductive plate;

each of said contact pads having an added conductive

layer on said metallization, said added layer having a conformal surface adjacent said chip and a planar outer surface, said outer surface suitable to form metallurgical bonds without melting;

said thermally conductive plate, attached to said active chip surface, having a thickness compatible with the thickness of said chip contact layers, and a surface suitable for metallurgical bonds; and

an assembly board having a plurality of planar, metallurgically bondable terminal pads in a distribution aligned with the distribution of said chip contact pads, and further having a thermally conductive site with a metallurgically bondable surface in a location aligned with the location of said chip plate;

said chip metallurgically bonded to said board so that each of said chip contact pads is connected to the corresponding board terminal pad, and said said plate is connected to said corresponding thermally conductive site.

26. A method for fabricating a semiconductor device having a semiconductor chip including a planar active surface and a metallization pattern including a plurality of contact pads, comprising the step of:

depositing at least one added conductive layer on said metallization of said contact pads, said added layer having a conformal surface adjacent said chip and a planar outer surface, said outer surface suitable to form metallurgical bonds without melting.

27. The method according to Claim 26 wherein said step of depositing is selected from a group consisting of sputtering, evaporating, and plating.

28. The method according to Claim 26 wherein said step of fabricating a planar outer surface of said added layer comprises the step of depositing said at least one added conductive layer by electroless plating.

29. The method according to Claim 26 wherein said step of fabricating a planar outer surface of said added layer comprises the step of depositing said at least one added conductive layer by screen printing.

30. The method according to Claim 26 wherein said step of fabricating a planar outer surface of said added layer comprises the step of depositing said at least one added conductive layer by using the method of support by islands of protective overcoat.

31. A method for fabricating a semiconductor assembly comprising the steps of:

providing a semiconductor chip having a planar active surface including an integrated circuit, said circuit having metallization patterns including a plurality of contact pads, each of said contact pads having an added conductive layer on said metallization, said added layer having a conformal surface adjacent said chip and a planar outer surface, said outer surface suitable to form metallurgical bonds without melting;

providing an assembly board having a plurality of planar, metallurgically bondable terminal pads in a distribution aligned with the distribution of said chip contact pads;

aligning said added chip metallization and said

board pads so that each of said chip contact pads is connected to a corresponding board terminal pad; and

metallurgically bonding said chip metallization and said board pads.

32. The method according to Claim 31 wherein said bonding comprises one of the following assembly techniques:

- direct welding by metallic interdiffusion;
- attaching including solder paste;
- attaching including a conductive adhesive.